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11-5-02

DOCKET NO. 122.1329/CJG

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Hisanori FUJISAWA

Serial No.: 09/045,041 Group Art Unit: 2123

Confirmation No.: 9340

Filed: March 20, 1998 Examiner: H. Jones

For: METHOD AND APPARATUS FOR CARRYING OUT CIRCUIT SIMULATION

RESPONSE AND REQUEST FOR EXAMINER INTERVIEW

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This is in response to the final Office Action mailed May 29, 2002, having a shortened period for response set to expire on August 29, 2002. A petition and fee for a two-month extension of time is enclosed, thereby extending the response period to October 29, 2002. A Request for Continued Examination is filed concurrently herewith. The following amendments and remarks are respectfully submitted.

REMARKS

Claims 9-12, 14-24, 26-36, and 38-44 are pending in this application and have been rejected. No new matter is being presented, and approval and entry are respectfully requested.

Rejections Under 35 U.S.C. §§ 102 and 103

On pages 2-6 of the Office Action, the Examiner rejected claims 9-12, 14-24, 26-36, and 38-44 under 35 U.S.C. §102(b) as being anticipated by Filseth (U.S. Patent No. 5,473,546); or Yokomizo et al. ("A New Circuit Recognition and Reduction Method for Pattern Based Circuit Simulation," IEEE Custom Integrated Cir. Conf., pp. 9.4/1-9.4/4); or Chakrabarti et al. ("An